S/N 09/945507 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner:

Son Dinh

Serial No.: 09

09/945,507

Group Art Unit:

2824

Filed:

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August 30, 2001

Docket:

1303.014US1

Title:

FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY

INSULATORS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

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Filing Date: August 30, 2001

Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 2nd day of February, 2004.

Name

Signatur

PTO/S8/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 09/945,507 Applicati n Number STATEMENT BY APPLICANT August 30, 2001 **Filing Date** (Use as many sheets as necessary) Forbes, Leonard **First Named Inventor Group Art Unit** 2824 Dinh, Son **Examiner Name** Attorney Docket No: 1303.014US1 Sheet 1 of 3

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EXAMINER

DATE CONSIDERED

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	09/945,507
(Use as many sheets as necessary)	Filing Date	August 30, 2001
	First Named Inventor	Forbes, Leonard
5 200 2	Group Art Unit	2824
Sheet 2 of 3	Examiner Name	Dinh, Son
Sheet 2 of 3	Attorney Docket No: 1	303.014US1

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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²		
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE	Complete if Known	
STATEMENT BY APPLICANT E	Application Number	09/945,507
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	First Named Inventor	Forbes, Leonard
FEB O 5 MON ON O	Group Art Unit	2824
FED S	Examiner Name	Dinh, Son
Sheet 3 of 3	Attorney Docket No: 1	303.014US1

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
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<u>S/N 09/945507</u> <u>PATENT</u>

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FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY

INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 09/945395	Filing Date August 30, 2001	Attorney Docket 1303.019US1	Title DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 09/945507

Filing Date: August 30, 2001

Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Dkt: 1303.014US1

10/075484	February 12, 2002	1303.043US1	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 2nd day of February, 2004.

Amy Moriarty